generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors;

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generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, said power-on reset signals having pulses not overlapping each other when threshold values of transistors formed in said semiconductor integrated circuit are typical values; and

initializing an internal circuit according to at least one of the pulses of said power-on reset signals. --

A marked-up copy of the amended claims is enclosed as required by 37 C.F.R. § 1.121.

REMARKS

The Office Action dated October 3, 2002 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. By this Amendment, claims 1, 3, 5, 7-11, 14 and 16 have been further amended to more clearly particularly point out and distinctly claim the invention. New claims 18-20 have been added. No new matter has been added. The Accordingly, claims 1-20 are pending in this application and are submitted for consideration.

Applicant respectfully acknowledges the courtesies extended to Applicant's representative during the personal interview on January 14, 2003. The points discussed during the interview are incorporated herein.

During the interview, the Examiner maintained his position with respect to the prior art rejection of claims 1-17. Applicant respectfully disagrees with the interpretation of the applied references discussed during the personal interview for the reasons set forth below.

Claims 8, 11, 14 and 16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. By this Amendment, the claims have been amended. Therefore, the rejection is requested to be withdrawn.

Claims 1-11 were rejected under 35 U.S.C. § 102(e) as being anticipated by Malherbe (U.S. Patent No. 6,252,442). However, Applicant submits that each of claims 1-11 recite subject matter that is neither disclosed nor suggested in the cited prior art.

Malherbe discloses an electronic circuit provided with a neutralization device that is designed to block the operation of any electronic circuit when the device is insufficiently supplied. The neutralization device of Malherbe is designed especially for electronic circuits supplied with low supply voltages. The device includes an upline with respect to an inhibiting means to block the operation of the electronic circuit, a control circuit reproducing the critical path or the potential critical paths of the functional electronic circuit in the form of elementary circuits. The deactivation of the inhibiting means is done only when the totality of the elementary circuits delivery same-state elementary signals indicating that the supply voltage is sufficient to ensure their efficient operation.

As is clear from Figs. 1 and 2 of Malherbe, there is only one triangular pulse generated in Malherbe. There are no rectangular pulses generated. In Malherbe, one of the logic levels (Low level in Malherbe) can be set with the triangular pulse, while the

other logic level (High level) is set in accordance with the threshold value.

However, in contrast, in amended claims 1, 3, 5 and 7-11 of the present invention recite that main power-on reset signals having at least one rectangular pulse is generated. With the rectangular pulses, both logic levels are set. Thus, in the present invention, the internal circuit can be initialized by making the difference between the low level and the high level of the main power-on reset signals large enough.

Additionally, amended claims 3 and 5 further disclose a reset terminal for receiving an external power-on reset signal. However, voltage detector DET is located inside toe semiconductor integrated circuit. Although the Office Action asserted that resistors 50 and 51 of voltage detector DET of Malherbe are means for providing an external power-on reset signal to amplifier 52, as discussed in col. 5, lines 13-14 of Malherbe, it is clearly stated that detector DET (Fig. 3) is provided in the control circuit CC. Thus, DET does disclose or suggest a reset terminal for receiving an external power-on reset signal.

Therefore, Malherbe fails to disclose a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals, as recited in claims amended claims 1, 3, 5 and 7-11.

Additionally, Malherbe fails to disclose or suggest a reset terminal for receiving an external power-on reset signal, as further recited in amended claims 3 and 5.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in amended claims 1, 3, 5 and 7-11, is not anticipated within the meaning of 35 U.S.C. § 102.

As for claims 2, 4 and 6, each of these claims depends on independent claims 1, 3 and 5, respectively. Therefore, each of these claims incorporates each and every limitation recited within claims 1, 3 and 5, respectively therein. Therefore, Applicant submits that each of claims 2, 4 and 6 also recites subject matter, which is neither disclosed nor suggested by Malherbe for at least the reasons set forth above with respect to claims 1, 3 and 5.

Claims 1-3, 5, 7, 8-12 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by Crotty (U.S. Patent No. 6,078,201). However, Applicant submits that each of amended claims 1-3, 5, 7, 8-11 and claims 12 and 17 recite subject matter that is neither disclosed nor suggested in the cited prior art.

Crotty discloses a power-on reset circuit for dual supply voltages. Fig. 2 of Crotty illustrates the power-on reset circuit 200, which includes a dual-voltage detection circuit 210 coupled to a first supply voltage terminal Vcc1, a second supply voltage terminal Vcc2, and a ground terminal. The dual-voltage detection circuit 210 determines whether supply voltage Vcc1 is greater than a first adequate voltage level Vad1 and in response outputs a first voltage detection signal VD1,. Circuitry coupled to second supply voltage terminal Vcc2 drives first voltage detection signal VD1 on output terminal 211. If first supply voltage Vcc1 is less than the first adequate voltage Vad1, the dual-voltage detection circuit 210 drives first voltage detection signal VD1 to a power-off logic level. If the first supply voltage Vcc1 is greater than the first adequate voltage Vad 1, the dual-voltage detection circuit 210 drives the first voltage detection signal VD1 to a power-on logic level.

However, the power-on reset signal POR in Crotty is not a pulse signal including

at least one rectangular pulse as in amended claims 1, 3, 5 and 7-11 of the present invention. This is clear from Figs. 4 and 5 of Crotty. In Fig. 4(a), the NAND gate 410 receives a VD1 and a delay signal which has the same logic as VD1. This is because the delay circuit in Crotty is formed to delete noises. Because of this, POR1 signal is not a pulse signal. This fact is also clear from the fact that there is an even number of inverters in the delay circuit of Fig. 5(a). Further, Fig. 7 in Crotty shows that since the buffer circuit 650 is an AND gate, POR signals having pulses cannot be generated from a POR1 signal.

Furthermore, as shown in Fig. 10 of Crotty does not show that the memory test circuit 1020 exists outside the semiconductor integrated circuit. Rather, Crotty indicates that the memory test circuit 1020 should exist inside the semiconductor integrated circuit. The POR3 signal that the memory test circuit 1020 outputs indicates whether or not the supply voltage is enough from the logic high and the logic low to be written into a memory cell (col. 11, lines 4-10). This means that the memory test circuit 1020 needs to be provided inside the semiconductor integrated circuit so that the supply voltage supplied to the semiconductor integrated circuit (or the internal supply voltage generated in the inside) can be directly detected. Therefore, the POR3 signal in Crotty appears to be generated inside the semiconductor integrated circuit. Thus, Crotty[1] does disclose or suggest a reset terminal for receiving an external power-on reset signal, as recited further recited in amended claims 3 and 5.

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[1] It is noted that Lee (U.S. Patent No. 5,394,104), which Crotty refers to in the specification also does not disclose the fact that the reset circuit exists outside the semiconductor integrated circuit.

Therefore, Crotty fails to disclose a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals, as recited in amended claims 1, 3, 5 and 7-11, or the main reset signal for generating a pulse, as recited in claims 12 and 17.

Additionally, Malherbe fails to disclose or suggest a reset terminal for receiving an external power-on reset signal, as further recited in amended claims 3 and 5.

As claims 2, 4 and 6, depends on independent claims 1, 3 and 5, respectively, it is respectfully submitted that each of these claims incorporates also recite subject matter which is neither disclosed nor suggested by Crotty for at least the reasons set forth above with respect to claims 1, 3 and 5.

Claims 13-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malherbe. However, Applicant submits that amended claims 14 and 16, and claims 13 and 15 are neither disclosed nor suggested in the cited prior art.

With respect to claims 13 and 15, as discussed above, voltage detector DET shown in Fig. 3 of Malherbe fails to disclose or suggest a reset terminal for receiving an external power-on reset signal. Thus, one of ordinary skill in the art would have been compelled to modify Malherbe by repositioning the detector.

With respect to amended claims 14 and 16, Malherbe fails to disclose or suggest wherein each pulse generator generates a respective pulse on the basis of a respective transition edge.

Still further as claims 14 and 16 depend from claims 13 and 15, respectively, Applicant respectfully submits that these claims are patentable for at least the same

reason as the independent claim.

Newly added claim 18 further recites that the main reset signal generator generates the main power-on reset signal having pulses respectively corresponding to each of the sub power-on reset signals, when threshold values of transistors formed in the semiconductor integrated circuit are typical values.

Newly added claim 19 further recites a reset terminal for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit, and a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to one of the sub power-on reset signal and the external power-on reset signal.

Newly added claim 20 further recites generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, the power-on reset signals having pulses not overlapping each other when threshold values of transistors formed in the semiconductor integrated circuit are typical values.

However, neither Malherbe, nor Crotty, alone or in combination discloses the above-discussed limitations. Therefore, it is respectfully submitted that newly-added claim 18-20 are also patentable over the prior art.

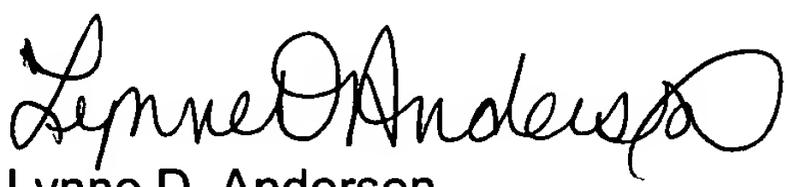
In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-20, and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referencing docket number 108397-00025.

Respectfully submitted,

ARENT FOX KINTNER PLOTKIN & KAHN PLLC



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Enclosures: Marked-up Copy of Claims
Petition for Extension of Time (two months)

MARKED-UP COPY OF CLAIMS

1. (Twice Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals.

3. (Twice Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal.

5. (Twice Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

7. (Twice Amended) A method of initializing a semiconductor integrated circuit

comprising the steps of:

generating a plurality of pulse signals as power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other, at least one of said pulse signals including a rectangular pulse; and

initializing an internal circuit according to at least one from any of said power-on reset signals.

8. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator, including [at least one transistor] transistors having [a] threshold [voltage] values, for generating a plurality of sub power-on reset signals on basis of the respective threshold [voltage] values of each of the transistors; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signals.

9. (Amended) A semiconductor integrated circuit comprising:

a first sub reset signal generator, including a first transistor having a first threshold voltage, for generating a first sub power-on reset signal on basis of the first threshold voltage;

a second sub reset signal generator, including a second transistor having a second threshold value, for generating a second sub power-on reset signal on basis of the second threshold voltage; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of the first sub power-on reset signal and the second sub

power-on reset signal.

10. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a plurality of pulse generators for generating pulses on basis of the plurality of sub power-on reset signals, respectively, at least one of said pulses being a rectangular pulse; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

11. (Amended) A method of initializing a semiconductor integrated circuit having a sub reset signal generator including transistors having threshold values, the method comprising the steps of:

generating a plurality of sub power-on reset signals, each according to ~~a~~ respective threshold [voltage] values of [a transistor] each of the transistors;

generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, at least one of said pulse signals including a rectangular pulse; and

initializing an internal circuit according to at least one of said power-on reset signals.

14. (Amended) A semiconductor integrated circuit according to claim 13, wherein said main reset signal generator comprises:

a plurality of pulse generators [for respectively generating pulses] , wherein each pulse generator generates a respective pulse on the basis of a respective transition

edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

16. (Amended) A semiconductor integrated circuit according to claim 15, wherein said main reset signal generator comprises:

a plurality of pulse generators [for respectively generating pulses], wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.